IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/174,164, filed June 17, 2002, ~~pending~~ now U.S. Patent 6,599,832, issued July 29, 2003, which is a divisional of application Serial No. 09/795,882, filed February 28, 2001, now U.S. Patent 6,410,420, issued June 25, 2002, which is a continuation of application Serial No. 09/136,384, filed August 19, 1998, now U.S. Patent 6,235,630, issued May 22, 2001.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] FIGS. 27-31 illustrate a common method of forming a cobalt silicide layer on an active-device region of a thin film semiconductor device. FIG. 27 illustrates an intermediate structure 400 comprising a semiconductor substrate 402 with a polysilicon layer 404 thereon, wherein the polysilicon layer 404 has at least one active-device region 406 formed therein with a thin dielectric layer 408, such as tetraethyl orthosilicate - TEOS, disposed thereover. The dielectric layer 408 must be as thin as possible to reduce the height of the thin film semiconductor device. A contact opening 412 is formed, by any known technique, such as patterning and etching, in the dielectric layer 408 to expose a portion of the active-device region 406, as shown in FIG. 28. A thin layer of cobalt 414 is applied over the dielectric layer 408 and the exposed portion of the active-device region 406, as shown in FIG. 29. A high temperature anneal step is conducted in an inert atmosphere to react the thin cobalt layer 414 with the active-device region 406 in contact therewith which forms a cobalt silicide layer 416, as shown in FIG. 30. However, dielectric materials, such as TEOS - tetraethyl orthosilicate, ~~BPSG~~ BPSG - borophosphosilicate glass, PSG - phosphosilicate glass, and BSG - borosilicate glass, and the like, are generally porous. Thus, the thin dielectric layer 408 has imperfections or voids which form passages through the thin dielectric layer 408. Therefore, when the high-temperature anneal is conducted, cobalt silicide also forms in these passages. The cobalt silicide structures in the passages are referred to as patches 418, as also shown in ~~FIG~~ FIG. 30. When the nonreacted

cobalt layer 414 is removed to result in a final structure 422 with a cobalt silicide layer 416 formed therein, as shown in FIG. 31, the patches 418 also form conductive paths between the upper surface of the thin dielectric layer 408 which can cause shorting and current leakage on IC backend testing devices which leads to poor repeatability and, thus, poor reliability of the data from the testing devices.

Please replace paragraph number **[0008]** with the following rewritten paragraph:

[0008] Although such voids can be eliminated by forming a thicker dielectric layer 424, the thicker dielectric layer 424 leads to poor step coverage of the cobalt material 426 in bottom corners 428 of the contact opening 412, as shown in FIG. 32. The poor step coverage is ~~cause~~ caused by a build-up of cobalt material 426 on the upper edges 432 of the contact opening 412 which causes shadowing of bottom corners 428 of the contact openings 412. The result is little or no cobalt material 426 deposited at the bottom corners 428 of the contact opening 412 and consequently an inefficient silicide contact formed after annealing.

Please replace paragraph number **[0036]** with the following rewritten paragraph:

[0036] Structures such as illustrated in FIG. 17 are generally used for testing of ~~flip-~~ flip-chips, wherein, as illustrated in FIG. 18, solder bumps 332 of a flip-chip 330 electrically contact the cobalt silicide layer 322. The cobalt silicide layer 322 conducts electrical signals to and/or receives electrical signals from the flip-chip 330 through the solder bumps 332.